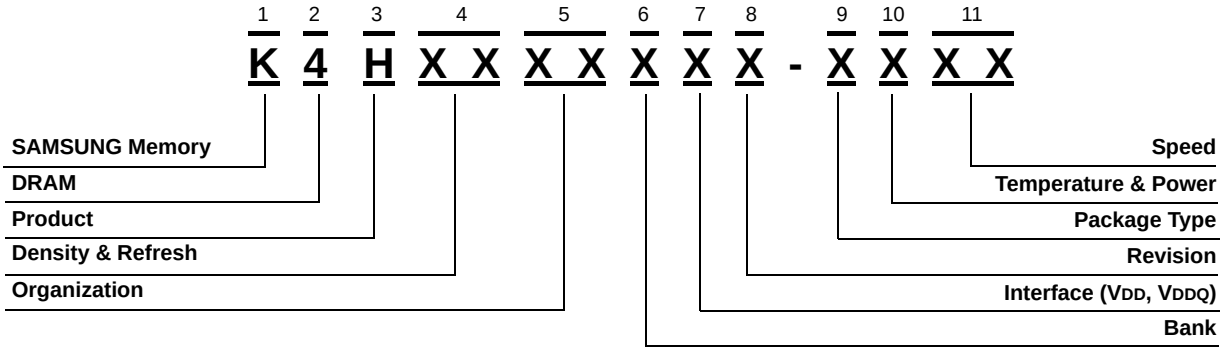
DDR SDRAM Product Guide

December 2007

Memory Division

A. DDR SDRAM Component Ordering Information



1. SAMSUNG Memory : K

2. DRAM : 4

3. Product

H : DDR SDRAM

4. Density & Refresh

28 : 128Mb, 4K/64ms
56 : 256Mb, 8K/64ms
51 : 512Mb, 8K/64ms
1G: 1Gb, 8K/64ms
2G: 2Gb, 8K/64ms

5. Organization

04 : x 4
06 : x 4 Stack
07 : x 8 Stack
08 : x 8
16 : x16

6. Bank

3 : 4 Banks

7. Interface (VDD, VDDQ)

8 : SSTL-2 (2.5V, 2.5V)

8. Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
G : 8th Gen.
H : 9th Gen.
J : 11st Gen.
N : 14th Gen.

9. Package Type

T : TSOP II
N : sTSOP II
G : FBGA
U : TSOP II (Lead-free)*1
V : sTSOP II (Lead-free)*1
Z : FBGA (Lead-free)*1
L : TSOP II (Lead-free & Halogen-free)*1
H : FBGA (Lead-free & Halogen-free)*1
F : FBGA for 64Mb DDR (Lead-free & Halogen-free)*1
6 : sTSOP II (Lead-free & Halogen-free)*1

Note 1: All of Lead-free or Halogen-free product are in compliance with RoHS

10. Temperature & Power

C : Commercial Temp.(0°C ~ 70°C) & Normal Power
L : Commercial Temp.(0°C ~ 70°C) & Low Power
I : Industrial Temp.(-40°C ~ 85°C) & Normal Power
P : Industrial Temp.(-40°C ~ 85°C) & Low Power

11. Speed

CC : DDR400 (200MHz @ CL=3, tRCD=3, tRP=3)
B3 : DDR333 (166MHz @ CL=2.5, tRCD=3, tRP=3)*1
A2 : DDR266 (133MHz @ CL=2 , tRCD=3, tRP=3)
B0 : DDR266 (133MHz @ CL=2.5, tRCD=3, tRP=3)

Note 1: "B3" has compatibility with "A2" and "B0"

B. DDR SDRAM Component Product Guide

Density	Bank	Part Number	Package*1 & Power*2 & Speed*3	Org.	Interface	Refresh	Power (V)	Package	Avail.
64Mb N-die	4Banks	K4H641638N	LCCC/CB3 LLCC/LB3	4M x 16	SSTL_2	4K/64m	2.5 ± 0.2V	66pinTSOPII	Now
			FCCC/CB3 FLCC/LB3					60ball FBGA	CS
256Mb H-die	4Banks	K4H560438H	UCA2/CB0 ULA2/LB0	64M x 4	SSTL_2	8K/64m	2.5 ± 0.2V*4	66pinTSOPII	Now
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H560838H	UCCC/CB3 ULCC/LB3	32M x 8				60ball FBGA	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H561638H	UCCC/CB3 ULCC/LB3	16M x 16				66pinTSOPII	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
256Mb J-die	4Banks	K4H560438J	LCB3/CB0 LLB3/LB0	64M x 4	SSTL_2	8K/64m	2.5 ± 0.2V*4	66pinTSOPII	CS
		K4H560838J	LCCC/CB3 LLCC/LB3	32M x 8				66pinTSOPII	CS
		K4H561638J	LCCC/CB3 LLCC/LB3	16M x 16				66pinTSOPII	CS
512Mb D-die	4Banks	K4H510438D	UCB0 ULB0	128M x 4	SSTL_2	8K/64m	2.5 ± 0.2V*4	66pinTSOPII	Now
			ZCCC ZLCC					60ball FBGA	
		K4H510838D	UCCC/CB3 ULCC/LB3	64M x 8				66pinTSOPII	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	
		K4H511638D	UCCC/CB3 ULCC/LB3	32M x 16				66pinTSOPII	
			ZCCC/CB3 ZLCC/LB3					60ball FBGA	

Note 1 :

U : TSOP II (Lead-free)
V : sTSOP II (Lead-free)
Z : FBGA (Lead-free)

L : TSOP II (Lead-free & Halogen-free)
H : FBGA (Lead-free & Halogen-free)
F : FBGA for 64Mb DDR (Lead-free & Halogen-free)
6 : sTSOP II (Lead-free & Halogen-free)

Note 2 :

C	Commercial Temperature, Normal Power
L	Commercial Temperature, Low Power

- Commercial Temp. (0°C <Ta< 70°C)

Note 3 :

	133Mhz	166Mhz	200Mhz
CL = 2	DDR266(A2)	-	-
CL = 2.5	DDR266(B0)	DDR333(B3)	-
CL = 3	-	-	DDR400(CC)

- "B3" has compatibility with "A2" and "B0"

Note 4 :

	DDR400	DDR333/266
VDD/VDDQ	2.6V ± 0.1V	2.5V ± 0.2V

C. Industrial temp DDR SDRAM Component Product Guide

Density	Bank	Part Number	Package*1 & Power*2 & Speed*3	Org.	Interface	Refresh	Power (V)	Package	Avail.
256Mb H-die	4Banks	K4H561638J	UICC/IB3/IB0 UPCC/PB3/PB0	16M x 16	SSTL_2	8K/64m	2.5 ± 0.2V*4	66pinTSOPII	Now
			ZIB3/IB0 ZPB3/PB0					60ball FBGA	
256Mb J-die	4Banks	K4H561638J	LICC/IB3 LPCC/PB3	16M x 16	SSTL_2	8K/64m	2.5 ± 0.2V*4	66pinTSOPII	CS
512Mb D-die	4Banks	K4H510838D	UIB3/IB0 UPB3/PB0	64M x 8	SSTL_2	8K/64m	2.5 ± 0.2V*4	66pinTSOPII	Now
			ZIB3/IB0 ZPB3/PB0					60ball FBGA	
		K4H511638D	UIB3/IB0 UPB3/PB0	32M x 16				66pinTSOPII	
			ZIB3/IB0 ZPB3/PB0					60ball FBGA	

Note 1 :

U : TSOP II (Lead-free)
V : sTSOP II (Lead-free)
Z : FBGA (Lead-free)

L : TSOP II (Lead-free & Halogen-free)
H : FBGA (Lead-free & Halogen-free)
F : FBGA for 64Mb DDR (Lead-free & Halogen-free)
6 : sTSOP II (Lead-free & Halogen-free)

Note 2 :

I	Industrial Temperature, Normal Power
P	Industrial Temperature, Low Power

- Industrial Temp. (-40°C <Ta< 85°C)

Note 3 :

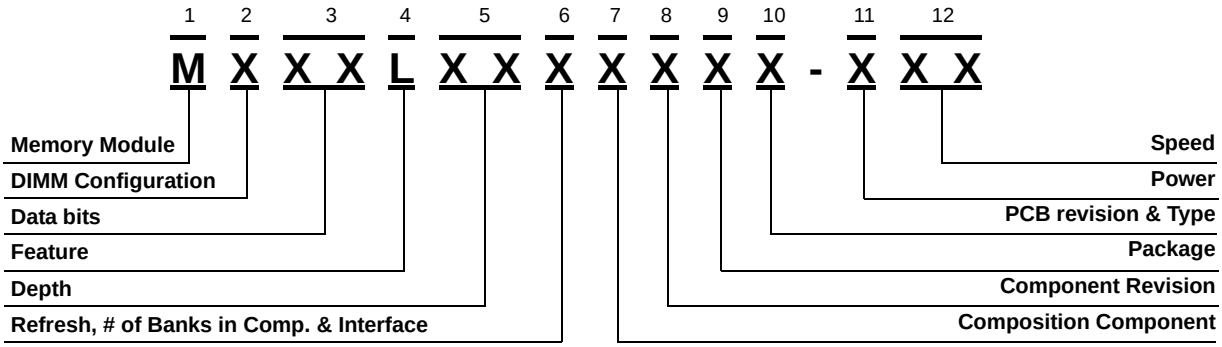
	133Mhz	166Mhz	200Mhz
CL = 2	DDR266(A2)	-	-
CL = 2.5	DDR266(B0)	DDR333(B3)	-
CL = 3	-	-	DDR400(CC)

- "B3" has compatibility with "A2" and "B0"

Note 4 :

	DDR400	DDR333/266
VDD/VDDQ	2.6V ± 0.1V	2.5V ± 0.2V

D. DDR SDRAM Module Ordering Information



1. Memory Module : M

2. DIMM Configuration

3 : DIMM
4 : SODIMM

3. Data Bits

68 : x64 184pin Unbuffered DIMM
81 : x72 184pin ECC unbuffered DIMM
83 : x72 184pin Registered DIMM
12 : x72 184pin Low Profile Registered DIMM
70 : x64 200pin Unbuffered SODIMM
63 : x64 172pin Micro DIMM

4. Feature

L : DDR SDRAM (2.5V VDD)

5. Depth

16 : 16M
32 : 32M
64 : 64M
28 : 128M
56 : 256M
51 : 512M
17 : 16M (for 128Mb/512Mb)
33 : 32M (for 128Mb/512Mb)
65 : 64M (for 128Mb/512Mb)
29 : 128M (for 128Mb/512Mb)
57 : 256M (for 512Mb)

6. Refresh, # of Banks in comp. & Interface

1 : 4K/ 64ms Ref., 4Banks & SSTL-2
2 : 8K/ 64ms Ref., 4Banks & SSTL-2

7. Composition Component

0 : x 4
3 : x 8
4 : x16
8 : x 4 Stack
9 : x 8 Stack

8. Component Revision

M : 1st Gen.
A : 2nd Gen.
B : 3rd Gen.
C : 4th Gen.
D : 5th Gen.
E : 6th Gen.
F : 7th Gen.
G : 8th Gen
H : 9th Gen.
J : 11th Gen.

9. Package

T : TSOP II (400mil)
N : sTSOP
G : FBGA
U : TSOP II*1 (Lead-Free)
V : sTSOP II*1 (Lead-Free)
Z : FBGA*1 (Lead-Free)

(Note 1 : All of Lead-free product are in compliance with RoHS)

10. PCB Revision & Type

0 : Mother PCB
1 : 1st Rev.
2 : 2nd Rev.
3 : 3rd Rev.
S : Reduced layer PCB

11. Temp & Power

C : Commercial Temp.(0°C ~ 70°C) & Normal Power
L : Commercial Temp.(0°C ~ 70°C) & Low Power

12. Speed

CC : DDR400 (200MHz @ CL=3, tRCD=3, tRP=3)
B3 : DDR333 (166MHz @ CL=2.5, tRCD=3, tRP=3)
A2 : DDR266 (133MHz @ CL=2 , tRCD=3, tRP=3)
B0 : DDR266 (133MHz @ CL=2.5, tRCD=3, tRP=3)

E. DDR SDRAM Module Product Guide

Org.	Den-sity	Part Number	Speed	Composition	Comp. Version	Voltage	Internal Banks	External Banks	PKG*1	Feature	Avail.
184Pin DDR Unbuffered DIMM											
32Mx 64	256MB	M368L3223HUS	CCC/CB3	32Mx 8 * 8pcs	256Mb H-die	2.5 ± 0.2V*3	4	1	66pin TSOP(II)	SS,1250mil	Now
		M368L3223JUS	CCC/CB3	32Mx 8 * 8pcs	256Mb J-die						
64Mx 64	512MB	M368L6423HUN	CCC/CB3	64Mx 8 * 16pcs	256Mb H-die			1		DS,1250mil	Now
		M368L6423JUN	CCC/CB3	64Mx 8 * 16pcs	256Mb J-die						
		M368L6523DUS*2	CCC/CB3	64Mx 8 * 8pcs	512Mb D-die					SS,1250mil	Now
128Mx 64	1GB	M368L2923DUN*2	CCC/CB3	64Mx 8 * 16pcs	512Mb D-die			2		DS,1250mil	Now
184Pin DDR Low Profile Registered DIMM											
64Mx 72	512MB	M312L6420HUS	CB0	64Mx 4 * 18pcs	256Mb H-die	2.5 ± 0.2V*3	4	1	66pin TSOP(II)	DS,1200mil	Now
		M312L6420JUS	CB0	64Mx 4 * 18pcs	256Mb J-die						
		M312L6523DZ3*2	CCC/CB3	64Mx 8 * 9pcs	512Mb D-die				60ball FBGA	SS,1125mil	Now
128Mx 72	1GB	M312L2920DUS*2	CB0	128Mx 4 * 18pcs	512Mb D-die			1	66pin TSOP(II)	DS,1200mill	Now
		M312L2923DZ3*2	CCC/CB3	64Mx 8 * 18pcs	512Mb D-die			2	60ball FBGA	DS,1125mil	Now
200Pin DDR SODIMM											
32Mx 64	256MB	M470L3224HU0	CB3	16Mx 16 * 8pcs	256Mb H-die	2.5 ± 0.2V*3	4	2	66pin TSOP(II)	DS,1250mi	Now
		M470L3224JU0	CB3	16Mx 16 * 8pcs	256Mb J-die						
64Mx 64	512MB	M470L6524DU0*2	CB3	32Mx 16 * 8pcs	512Mb D-die						Now
128Mx 64	1GB	M470L2923DV0*2	CB3	64Mx 8 * 16pcs	512Mb D-die				54pin sTSOP(II)		Now

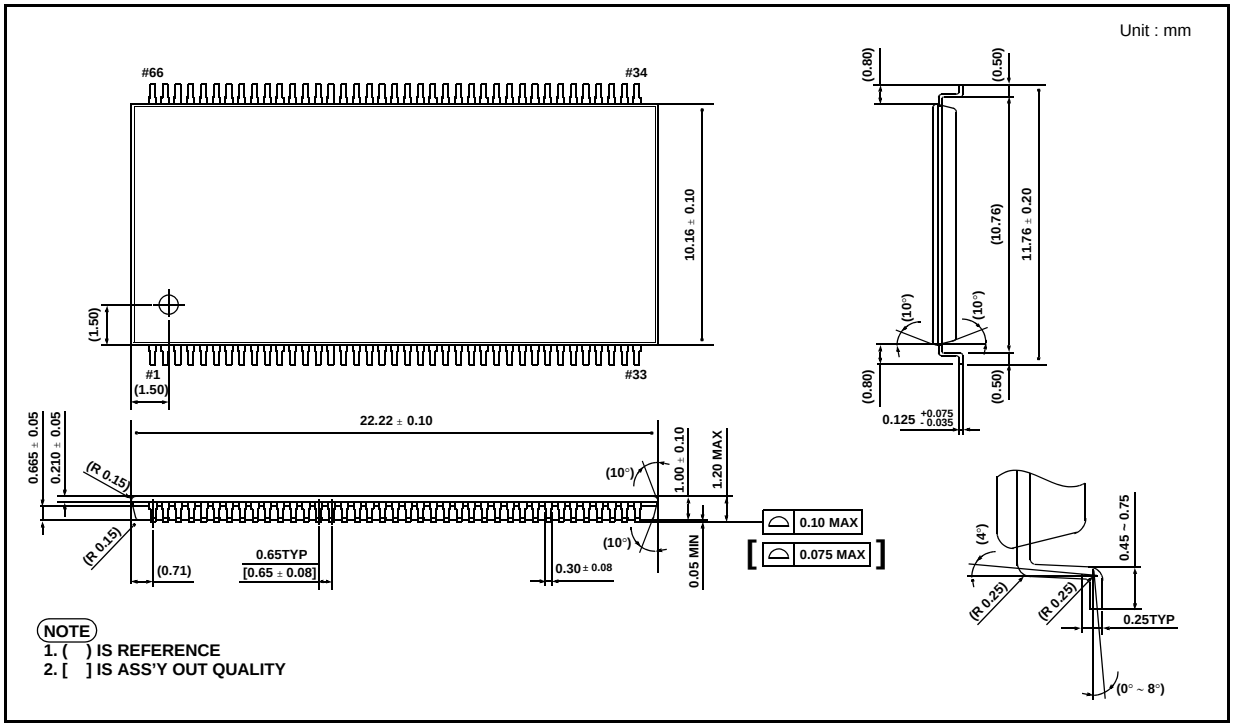
Note 1 : **(All of DDR DIMMs can support Lead-free)**
U : TSOP II (Lead-Free)
V : sTSOP II (Lead-Free)
Z : FBGA (Lead-Free)

Note 2 : All of DDR components support both Leaded and Lead-free. And 256Mb H-die, J-die and 512Mb D-die Lead-free is default PKG Type.

Note 3 :

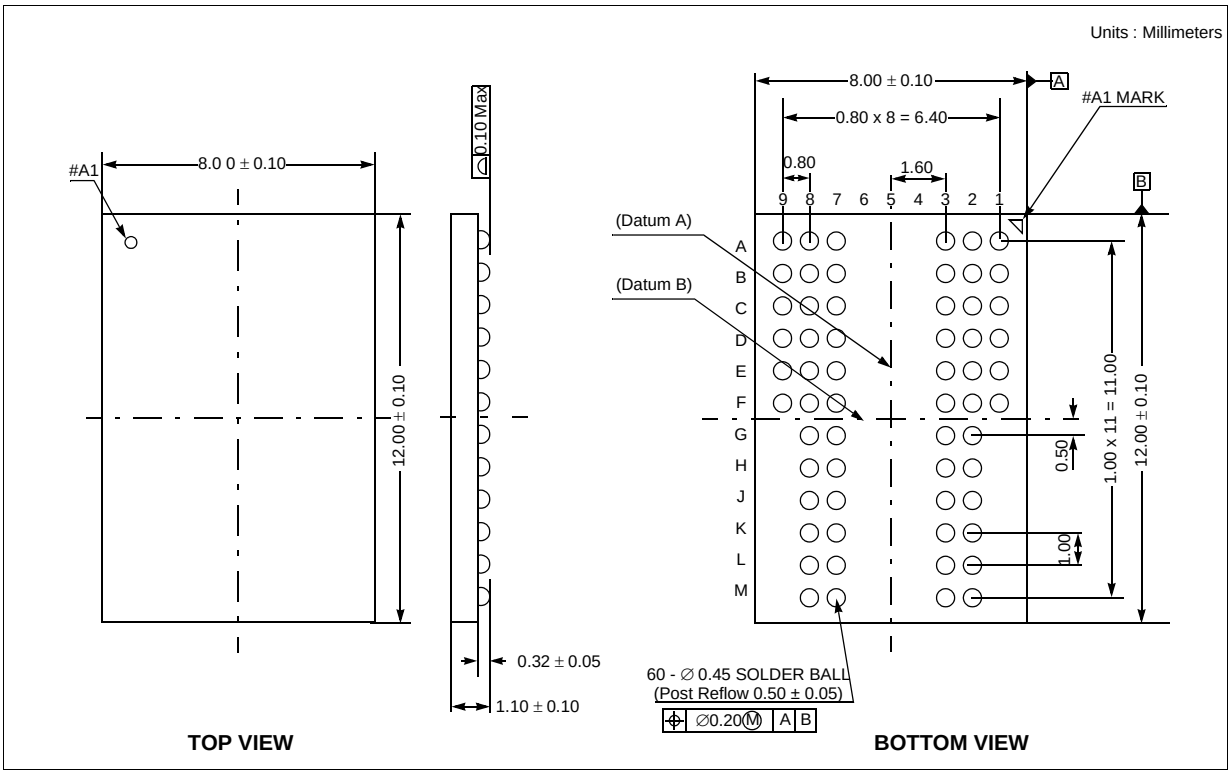
	DDR400	DDR333/266
VDD/VDDQ	2.6V ± 0.1V	2.5V ± 0.2V

F. Package Dimension

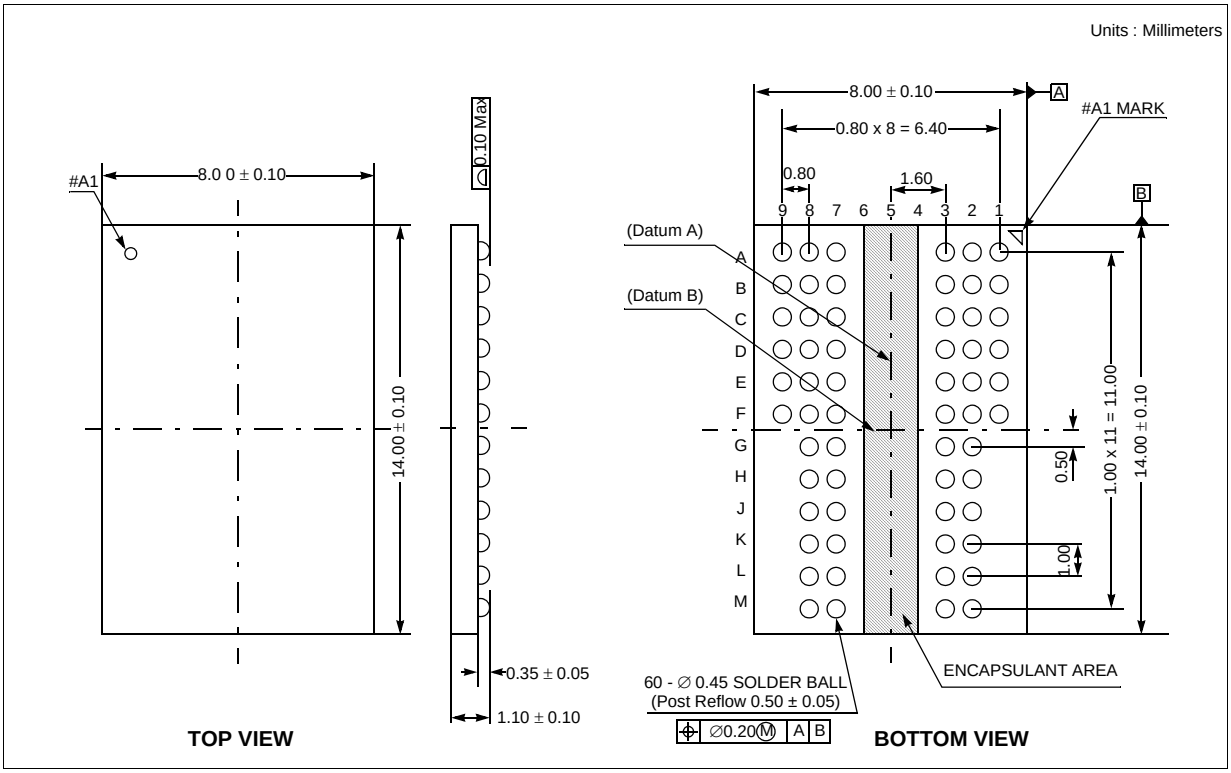


66Pin TSOP(II) Package Dimension

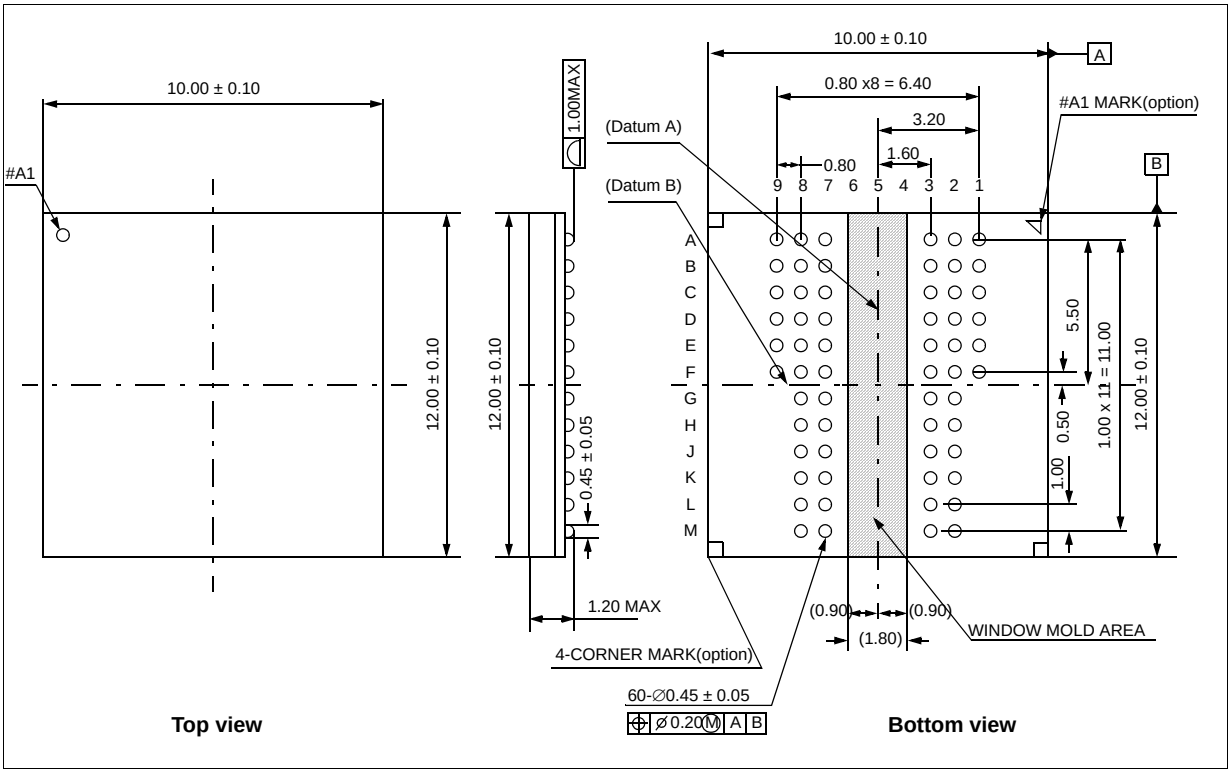
60Ball FBGA (For 64Mb)



60Ball FBGA (For 256Mb)



60Ball FBGA (For 512Mb)



For further information,

semiconductor@samsung.com